CLAIMS

What is claimed:

1. A method, comprising:

calculating a variation between an input data rate and a pre-determined output data rate, the input data rate being based on a number of data read requests; and

compensating for the variation by modifying the number of data read requests.

2. The method of claim 1, wherein the variation is compensated to increase a bandwidth in a communication channel.

3. The method of claim 1, wherein the variation is compensated to increase the bandwidth in a plurality of communication channels.

4. The method of claim 1, wherein the variation is compensated to decrease a number of idle cell insertions.

5. The method of claim 1, wherein modifying the number of data read requests comprises generating additional data read requests.

6. The method of claim 1, wherein modifying the number of data read requests comprises masking data read requests.

7. The method of claim 1, wherein calculating the variation further comprises:

determining a difference between a total bit group of data received from an input first-in-first-out (FIFO) and a pre-determined output data bus width;

subtracting the difference from a counter value;

masking a data read request transmitted from a packet encapsulator to the input FIFO when the counter value is at least equal to and less than a negative value of the pre-determined output data bus width; and

generating an additional data read request to be transmitted from the packet encapsulator to the input FIFO when the counter value is at least equal to and greater than a positive value of the pre-determined output data bus width.

8. The method of claim 1, wherein calculating the variation further comprises:

determining a difference between a total bit group of data received from an input first-in-first-out (FIFO) and a pre-determined output data bus width;

subtracting the difference from a counter value;

masking a data read request transmitted from a packet encapsulator to the input FIFO when the counter value is at least equal to and greater than a positive value of the pre-determined output data bus width; and

generating an additional data read request to be transmitted from the packet encapsulator to the input FIFO when the counter value is at least equal to and less than a negative value of a pre-determined output data bus width.

9. The method of claim 1, further comprising:

transmitting an output data stream to an output first-in-first-out (FIFO);

determining when the output FIFO is substantially full;

passing the data read requests to an input FIFO when the output FIFO is not substantially full; and

masking the data read request to the input FIFO when the output FIFO is substantially full.

10. The method of claim 8, wherein substantially full is determined using a number of stages of pipeline subtracted from a capacity of the output FIFO.

11. The method of claim 1, further comprising:

comparing a total bit group of data received by a packet encapsulator from a data read request with a counter value; and

performing at least one of masking a data read request and generating an additional data read request.

12. The method of claim 11, wherein the total bit group of data is a byte.

13. The method of claim 11, further comprising passing the data read request to an input first-in-first-out (FIFO).

14. The method of claim 11, further comprising passing the data read request and the additional data read request to an input first-in-first-out (FIFO).

15. An apparatus, comprising:

an encapsulator engine; and

a packet pre-processor coupled to the encapsulator engine, the packet pre-processor to calculate a variation between an input data rate and a pre-determined output data rate, the input data rate being based on a number of data read requests, the packet pre-processor to compensate for the variation by modifying the number of data read requests.

16. The apparatus of claim 15, wherein packet pre-processor comprises:

a pre-compute circuitry to calculate a total bit group of data received by the packet pre-processor at the input data rate; and

a request modifier circuitry coupled to the pre-compute circuitry, the request modifier circuitry to determine a difference between the total bit group of data calculated by the pre-compute circuitry and a pre-determined output data bus width.

17. The apparatus of claim 16, further comprising:

a link layer device;

an input first-in-first-out (FIFO) coupled to the request modifier circuitry, link layer device and the pre-compute circuitry, the input FIFO to receive input data at the input data rate; and

an output FIFO coupled to the encapsulator engine and the request modifier circuitry, the output FIFO to transmit output data at the pre-determined output data rate.

18. The apparatus of claim 17, further comprising:

a framer engine coupled to the output FIFO; and

a physical interface device coupled to the framer engine.

19. The apparatus of claim 18, wherein the pre-compute circuitry receives input data from the input FIFO, the encapsulator engine receives the input data from the pre-compute circuitry, the output FIFO receives the output data from the encapsulator engine, the request modifier circuitry receives data read requests from the framer engine, the link layer device receives the data read requests from the request modifier circuitry.

20. An apparatus, comprising:

means for transmitting data through a communication channel having a bandwidth;

means for modifying data read requests transmitted by a framer engine; and

means for increasing a utilization efficiency of the bandwidth.

21. The apparatus of claim 20, further comprising means for decreasing a number of idle cell insertions.

22. The apparatus of claim 20, further comprising means for compensating for invalid bytes of an input data stream.

23. A system, comprising:

a link layer device;

a first physical interface device; and

a framer coupled to the link layer device and the first physical interface device, wherein the framer comprises an encapsulator engine and a packet pre-processor coupled to the encapsulator engine, the packet pre-processor to calculate a variation between an input data rate and a pre-determined output data rate, the input data rate being based on a number of data read requests, the packet pre-processor to compensate for the variation by modifying the number of data read requests.

24. The system of claim 23, wherein the packet pre-processor comprises:

a pre-compute circuitry to calculate a total bit group of data received by the packet pre-processor at the input data rate; and

a request modifier circuitry coupled to the pre-compute circuitry, the request modifier circuitry to determine a difference between the total bit group of data calculated by the pre-compute circuitry and a pre-determined output data bus width.

25. The system of claim 24, further comprising a second physical interface device coupled to the link layer device, wherein the second physical interface device, the link layer device, the framer and the first physical interface device reside in a line card.

26. The system of claim 25, wherein the second physical interface device is an Ethernet device and the first physical interface device is a Synchronous Optical Network (SONET) device.

27. The system of claim 25, wherein the line card is coupled to a wide area network (WAN).